

REMARKS

Claims 1-54 are pending in the above-identified application. Claims 1, 2, and 45 are argued in the Office Action. Claim 1 is independent. Claims 3-44, 46-54 have been withdrawn from consideration.

Comments on Restriction Requirement

Applicant notes that species III was alleged in the restriction requirement as corresponding to Figure 4. Applicant notes that claims 10 and 18 correspond to Figure 4 (e.g., including current control switch 13), and accordingly requests that claims 10 and 18 be included in the set of elected claims. Thus, in addition to claims 1, 2, and 45, Applicant respectfully requests that claims 10 and 18 be examined as being drawn to species III.

Claim Rejection – 35 U.S.C. 102

Claims 1, 2, and 45 have been rejected under 35 U.S.C. 102(b) as being anticipated by Iwata (U.S. Patent 6,049,252). Applicant respectfully traverses this rejection.

Summary of the Present Invention

The present invention, in a preferred embodiment, is directed to a variable gain amplifier for use in broadband wireless communication devices. An advantage of the variable gain amplifier of the present invention is that it is of small mount area and is operable to compensate for a decrease of a gain by

an increase of an IIP3. IIP3 (third-order Input Intercept Point) is an index of the third-order distortion component of the circuit, and is an input value at which the third-order intermodulation component in response to a two-tone input takes the value of the first-order component (Specification: page 5, lines 7-12).

The Variable gain amplifier in general includes an amplifying transistor section and a current path control circuit, which controls a current path through the amplifying transistor section. Voltage V_{od} which determines the IIP3 of the transistor is given by

$$V_{od} = \{ I / (K * W / L) \}^{1/2}$$

Transconductance g_m which determines the gain of the transistor can be determined by differentiating the current through the transistor as follows

$$g_m = 2 * \{ I * K * W / L \}^{1/2}$$

Based on these relationships, when the size W/L of the transistor is decreased by the current control circuit under current I held at a constant value, the voltage V_{od} is increased, and the transconductance g_m is decreased. When the size W/L of the transistor is increased, the voltage V_{od} is decreased and the transconductance g_m is increased. By making the size of the transistor smaller or larger under constant current flowing through the amplifying transistor, the variable gain amplifier increases or decreases the IIP3 (Specification: page 13).

Specifically, the variable gain amplifier is arranged such that when the size of the amplifying transistor is decreased or increased under constant current maintained by a current path control section, the IIP3 is increased or

decreased and the gain is decreased or increased. In short, a variable gain amplifier is provided that is capable of compensating for a decrease of the gain by an increase of the IIP3. Further, with a current control transistor (e.g. 12, Figure 2) in the current path control, the current path through the amplifying transistor can be independently controlled (Specification: page 14, line 21, to page 15, line 13).

Iwata

Iwata is directed to a programmable-gain amplifier in which fine and linear gain control can be realized with a simple circuit configuration. The programmable-gain amplifier includes a cascade connection of differential amplifiers (E1 to En) and a current controller (100). The current controller has a current mirror circuit.

In Iwata, the amplification factor of each differential amplifier is varied in proportion to the emitter current supplied to each differential amplifier. Thus, gain control is realized by controlling current values of the first to the n-th emitter currents by the current controller (Iwata, column 3, lines 57-63).

Iwata also discloses that by changing a logic level set of binary control signals to be supplied to the control terminals, a product of current values of the emitter currents, which defines the total gain of the programmable-gain amplifier, can be controlled (Column 4, lines 35-41). Thus, by designing the relative on-resistance of each of the MOS transistors (e.g., M_0) to be in inverse proportion to the relative emitter size of respective bi-polar transistors,

(e.g., Q_0) current values of the emitter current can be controlled (Column 4, lines 42-65).

Differences over Iata

Claim 1 is directed to a variable gain amplifier comprising an amplifying transistor and a current path control section. The Office Action alleges that Iwata's differential amplifier (E1) teaches the claimed amplifying transistor and that Iwata's current controller (100) teaches the claimed current path control section. Applicant disagrees that current controller of Iwata teaches at least the claimed "current path control section which controls a size of the amplifying transistor."

Iwata does appear to teach designing the relative emitter size of the input, the output and the control bi-polar transistors Q_0 to Q_n and Q_{cl} to Q_{cm} . In particular, an amplifier controls the emitter size (i.e., amount of current) of the transistors of the current controller (current controlling section) 100 which controls the amounts of currents supplied to the differential amplifiers. The amounts of currents from the current controlling section to the differential amplifiers E_1 , E_2 , ... are controlled so that the amplification factor is varied. Gain control is then realized by controlling current values of emitter currents by the current controller.

In other words, the sizes of the respective differential amplifiers E_1 , E_2 , ... and current paths through these amplifiers are always constant. Only the sizes and current paths of the transistors in the current controlling section vary. Current paths through the transistors of the differential amplifiers are not

controlled by the current controller section. Size of transistors of the differential amplifiers are not controlled. Thus, at least for this reason, Applicant submits that each and every claimed element of claim 1 is not taught in Iwata. Further, this argument applies as well to dependent claims 2 and 45.

Further with respect to claim 45, the claim is directed to a current flow through the amplifying transistor maintained at a constant level when the amplification factor is varied. Iwata, on the other hand, discloses that control signals supplied to terminals CTL₁ and CTL₂ cause a current supplied to the amplifying transistor E₁ to precisely vary as 40μA, 42μA, 44μA, and 46μA (for example, as can be seen in Figure 3).

Accordingly, Applicant respectfully requests that the rejection be withdrawn.

CONCLUSION

In view of the above amendments and remarks, reconsideration of the various rejections and allowance of claims 1, 2, and 45 is respectfully requested.

Should the Examiner have any questions concerning this application, the Examiner is invited to contact Robert W. Downs (Reg. No. 48,222) at (703) 205-8000 in the Washington, D.C. area.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit

Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully Submitted,

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